REMARKS

In response to the Office Action mailed October 17, 2003, Claims 1-5 and 7-20 were examined and rejected. In response Claims 1 and 11 are amended, Claims 2-3 and 13-14 are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1, 4-5, 7-12 and 15-20, as amended, in view of at least the following remarks.

I. Claims Rejected Under 35 U.S.C. §103

The Patent Office rejects claims 1-5 and 7 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,599,734 issued to Byun, et al. ("Byun") in view of Kroner, et al. (IEEE 2000) ("Kroner"). Applicants respectfully traverse this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP 2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Claims 1 and 11

Applicants have amended Claims 1 and 11 to include the following:

> forming a SOG layer containing impurities, including one of a p-type impurity and an n-type impurity on the entire surface of the semiconductor substrate by spin-coating and densifying a liquid silicate glass including one of P, B, In, As, and Sb doping elements. [Emphasis added]

Applicants respectfully submit that these features of Claims 1 and 11 are neither taught nor suggested by either Byun or Kroner. Namely, according to Byun,

> A disposable layer 24 having a first conductivity type impurity and a second conductivity impurity of a higher concentration than that of the first conductivity impurity is formed over the entire surface of the substrate by CVD process, as shown in FIG. 2B, and then the resultant structure is subjected to an anneal treatment such as rapid thermal annealing or furnace so that a highly doped source/drain area of a shallow junction can be formed (FIG. 2C). (Col. 3, lines 33–40) [Emphasis added]

Hence, the SOG layer of Claim 1, as amended, is formed by spin-coating a liquid silicate glass, densifying the liquid silicate glass and removing a solvent in the liquid silicate glass. Conversely, the BPSG layer of Byun is formed by chemical vapor deposition (CVD). Conventionally, a BPSG layer is formed by decomposing a composition gas including a silicon-oxygen source gas, e.g., TEOS ($Is(OC_2H_5)_4$, Tetra OrthoSilicate) and dopant gases, e.g., PH_3 and B_2O_6, using CVD.

Accordingly, the SOG layer and the BPSG layer are quite different in the fabrication step. According to the Examiner, forming of the SOG layer by spin-coating and densifying a liquid silicate glass including one of P, B, In, As, and Sb doping elements is taught by Byun at col. 3, lines 38-57 and FIG. 2B. Namely:

> This embodiment employs BPSG layer as the disposable layer 24, where, when n type silicon substrate 21 is used or p type MOS transistor is made, the BPSG layer is substantially B+PSG layer 24 being doped with a higher dopant concentration of boron than that of phosphorus, in which B+PSG layer is doped with the dosage of 5E21 atoms/cm^2 for boron and 1E21 atoms/cm^2 for phosphorous. Meanwhile, when p type silicon substrate 11 is used or n type MOS transistor is fabricated, the BPSG layer is substantially BP+SG layer 24 being doped with a higher dopant concentration of phosphorous than that of boron, in which BP+SG layer is doped with the dosage of 1E21 atoms/cm^2 for boron and 5E21 atoms/cm^2 for phosphorous. It is noted that a layer of B+PSG means BPSG layer being doped with a higher dopant concentration of boron than that of phosphorus, while a layer of BP+SG means BPSG layer being doped with a higher dopant concentration of phosphorus that that of boron.

However, after careful review of the cited passage, Applicants must disagree with the Examiner's contention since the cited passage contains no reference to forming of the SOG layer by spin-coating and densifying a liquid silicate glass including one of P, B, In, As, and Sb doping elements, as required by Claims 1 and 11. Furthermore, as correctly pointed out by the Examiner, Byun fails to provide any teachings or suggestions with regards to the additional implanting of impurity ions into the SOG layer to increase the concentration of impurities in the SOG layer. However, according to the Examiner,

> It would have been obvious to one of ordinary skill in the art of making a semiconductor devices to combine teachings of Kroner and Byun to enable the process of additionally implanting impurity ions into portions of the SOG layer formed on the diffusion barrier layer and the semiconductor substrate by a plasma ion implantation of Byun to be performed and furthermore to increase the concentration of impurities in the SOG layer because it is a doping method for high does and low energy implants. (pg. 476, Abstract.)

Applicants respectfully disagree with the Examiner's contention. In fact, Applicants respectfully submit that the teachings of Kroner are limited to only implanting impurity ions into a silicon layer or a polysilicon layer using an Ion Shower Implanter, as illustrated by FIGS. 1 and 5 of Kroner.

In contrast, Claims 1 and 11, as amended, require:

> additionally implanting impurity ions into portions of the SOG layer formed on the diffusion barrier layer and the semiconductor substrate to increase the concentration of impurities in the SOG layer. [Emphasis added]

Moreover, even assuming that one skilled in the art modified Byun in view of Kroner, Applicants respectfully submit that the teachings of modification would be limited to ion shower

implantation directly into the substrate 21 (with or without a layer of polysilicon), prior to formation of disposable layer 24. Hence, Kroner does not explicitly disclose additional implanting impurity ions into the SOG layer in order to increase the concentration of impurities in the SOG layer, as required by Claims 1 and 11. Furthermore, the Examiner fails to illustrate any motivation for combining Byun with Kroner. Accordingly, the combining of Byun in view of Kroner is not proper since the combination is based on improper, hindsight-based analysis. As a result, the modification proposed by the Examiner fails to teach additionally implanting impurity ions into portions of the SOG layer formed on the diffusion barrier layer and the semiconductor substrate to increase the concentration of impurities in the SOG layer, as required by amended Claims 1 and 11.

Accordingly, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claims 1 and 11, since the combination of the references cited by the Examiner fail to teach or suggest all the claim limitations and, specifically, the additional impurity implantation into portions of the SOG layer. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 1 and 11.

Claims 4-5 and 7-10

Claims 4-5 and 7-10 depend from Claim 1 and, therefore, include the patentable claim limitations of Claim 1, as described above. Consequently, Claims 4-5 and 7-10, based on their dependency from Claim 1, are patentable over the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 4-5 and 7-10.

Claims 15-20

Claims 14-20 depend from Claim 11 and, therefore, include the patentable claim limitations of Claim 11. As a result, Claims 15-20, based on their dependency from Claim 11, are patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 15-20.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1, 4, 5, 7-12 and 15-20 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 14, 2004

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Marilyn Bass January 14, 2004